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First Named Inventor	Pai-Hung Pan
Art Unit	2823
Examiner Name	G. Fourson III
Attorney Docket Number	2269-2919.4US (96-0499.01/US)

ENCLOSURES ***(check all that apply)***

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
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- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Brief in response to Notification of Non-Compliant Appeal Brief dated August 11, 2006
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) *(please identify below)*:

Remarks

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 AND 1.17 TO Deposit Account 20-1469 during pendency of this application.

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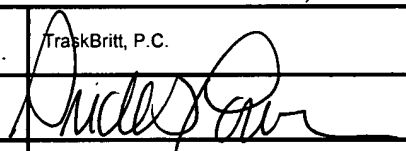
Signature			
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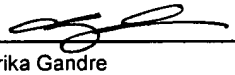
Signature			
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Pai-Hung Pan

Serial No.: 09/072,959

Filed: May 5, 1998

For: TECHNIQUE FOR FORMING SHALLOW TRENCH ISOLATION STRUCTURE WITHOUT CORNER EXPOSURE AND RESULTING STRUCTURE

Confirmation No.: 7136

Examiner: G. Fourson III

Group Art Unit: 2823

Attorney Docket No.: 2269-2919.4US
(96-0499.01/US)

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APPEAL BRIEF

Mail Stop Appeal Brief – Patents
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Attn: Board of Patent Appeals and Interferences

Sir:

This APPEAL BRIEF is being submitted in the format required by 37 C.F.R. § 41.37(c)(1).

I. REAL PARTY IN INTEREST

U.S. Serial No. 09/072,959 (hereinafter "the '959 Application), the application at issue in the above-referenced appeal, is assigned to Micron Technology, Inc. The assignment was recorded with the United States Patent & Trademark Office (hereinafter the "Office") Reel 8618, Frame 0703. Accordingly, Micron Technology, Inc. is the real party in interest to the above-referenced appeal.

II. RELATED APPEALS AND INTERFERENCES

The final rejections that were presented in U.S. Application Serial No. 09/944,506, which was filed on August 30, 2001, are currently the subject of an appeal before the Board of Patent Appeals and Interferences (hereinafter "the Board"), an Appeal Brief having been filed on June 7, 2005.

Neither appellants nor the undersigned attorney are aware of any other appeals, interferences, or any other actions that are currently ongoing before Board or any federal court that may affect or be affected by the decision of the Board on this appeal of the final rejections of the claims of the '959 Application.

III. STATUS OF CLAIMS

Claims 1-5, 11-17, 25-28, and 33-38 remain pending in the '959 Application. The Examiner continues to reject each of these claims. Accordingly, the final rejections of claims 1-5, 11-17, 25-28, and 33-38 are being appealed.

IV. STATUS OF AMENDMENTS

The '959 Application was filed on May 5, 1998, with fifty-two (52) claims. Claims 6-10, 18-24, 29-32, and 39-52, which were already being pursued in a parent of the '959 Application, were canceled in a Preliminary Amendment that was filed with the '959 Application.

A first Office Action on the merits was mailed on November 12, 1999.

In response, an Amendment was filed on February 14, 2000.

In view of the arguments that were presented in the Amendment of February 14, 2000, the Office withdrew its previous rejections and presented several new rejections in a second, nonfinal Office Action, which was sent on April 25, 2000.

Another amendment, in which minor revisions were made to the claims merely for the sake of clarity, was filed on July 24, 2000.

In reply, the Office mailed a third, final Office Action on October 11, 2000, maintaining each prior art rejection that was presented in the Office Action of April 25, 2000.

An Amendment Under 37 C.F.R. § 1.116 was filed on December 19, 2000, in which further clarifying amendments were made to the claims.

The Office refused to enter and consider the claim amendments, issuing an Advisory Action on January 4, 2001, in which the latest grounds for rejecting the claims on the basis of subject matter disclosed in the prior art were preserved.

In order to have the claims considered, a Continued Prosecution Application (CPA) was filed on January 11, 2001.

A fourth Office Action on the merits followed on March 30, 2001. In the fourth Office Action, the Office continued to assert each of the previously presented prior art rejections.

On July 2, 2001, another Amendment, in which further clarifications were made in the claims, was filed.

A fifth, final Office Action was mailed on October 11, 2001. Again, the Office maintained each of its previously presented prior art rejections.

Another Amendment Under 37 C.F.R. § 1.116 was mailed on December 11, 2001.

The Office refused to accept the reasoning that was presented in the December 11, 2001, Amendment Under 37 C.F.R. § 1.116, issuing an Advisory Action on January 7, 2002.

Thereafter, on January 16, 2002, a Request for Continued Examination (RCE) was filed.

On April 9, 2002, the Office mailed a sixth Office Action, in which claims 11-17 and 33-38 were allowed. The prior art rejections of the remaining claims were, however, maintained.

Further explanations as to the patentability of the claims that remained rejected were provided in a Response dated July 16, 2002.

A seventh, nonfinal Office Action was sent on October 24, 2002. The Office withdrew its allowance of claims 11-17 and 33-38, reinstating its prior art rejections of these claims and maintaining each of the prior art rejections that remained.

On January 29, 2003, another Amendment was filed. A few more minor claim amendments were presented to further clarify the subject matter that was already recited in the amended claims. In addition, reasoning was provided to clearly explain the patentability of each of the pending claims.

Nonetheless, each of the pending claims was again rejected in an eighth, final Office Action dated April 8, 2003. Again, the Office asserted each of the prior art rejections that it had been asserting since April 25, 2000.

In a Response to the Final Office Action, which was filed on June 13, 2003, another effort was made to convince the Office that each of claims 1-5, 11-17, 25-28, and 33-38 recites subject matter which is allowable over the prior art that has been made of record in the '959 Application.

In an Advisory Action dated July 15, 2003, the Office indicated its intent to continue its refusal to accept the explanations of patentability. In response, a Notice of Appeal was filed on July 18, 2003, and an Appeal Brief followed on September 18, 2003.

Thereafter, on June 28, 2004, an Examiner's Answer to the Appeal Brief was issued.

On Monday, August 30, 2004, a Request for Continued Examination (RCE) was filed along with an Amendment, in which further claim revisions were presented. Following the receipt of a Notice of Non-Compliant Amendment, a Supplemental Amendment was mailed on October 7, 2004. Not further amendments have been made to the claims of the '959 Application.

A ninth, non-final Office Action followed on December 28, 2004. In the ninth Office Action, the Examiner revised his grounds for rejecting the pending claims.

Explanations as to the patentability of the claims over the art upon which the new rejections were based were provided in a Response dated April 28, 2005.

In a Final Office Action dated June 22, 2005, the Examiner rejected Appellants' reasoning, which was subsequently reiterated in Response mailed on August 10, 2005.

The final rejections of the pending claims were maintained in an Advisory Action that was issued on August 30, 2005.

Unable to convince the Examiner that the pending claims are patentable over the art of record, Appellants filed a Notice of Appeal on September 6, 2005. The Notice of Appeal is followed by this Appeal Brief, which is being filed on Monday, November 7, 2005, and should be deemed to have been filed within two months of the filing date of the Notice of Appeal, as November 6, 2005, fell on a Sunday. 37 C.F.R. § 1.7.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claims of the '959 Application are directed to methods for forming isolation structures for semiconductor devices. In such a method, a layered structure which includes a semiconductor substrate, a dielectric layer, and a buffer film layer may be provided. Independent claims 1 and 11; Fig. 1; page 4, lines 13-22; page 6, lines 15-25. The layered structure may be etched to define a trench which extends through the buffer film layer, through the dielectric layer, and into the semiconductor substrate. Independent claims 1 and 11; Figs. 2 through 4; page. 4, lines 23-27; page 6, line 26, to page 7, line 7. The trench may include sidewalls and a bottom. Independent claims 1 and 11; *see, e.g.,* Fig. 4.

An oxide layer may be formed on portions of the semiconductor substrate that are exposed within the trench. Independent claims 1 and 11; Fig. 5; page 5, lines 1-3; page 7, lines 8-11. Thermal oxidation processes may be used to form the oxide layer. Claim 2; page 5, lines 1-3; page 7, lines 8-11.

A portion of the buffer film layer may be selectively etched. Independent claims 1, 11, 25, and 33; Fig. 6; page 5, lines 3-5; page 7, lines 11-16. Such selective etching may expose portions of an upper surface of the dielectric layer that are located adjacent to an upper edge of

the trench. *see* Fig. 6. Some of the buffer film layer may remain on the semiconductor substrate following such selective etching. *See id*; claims 4, 14, 27, and 35.

Isolation material may be applied over the buffer film layer (independent claims 1, 11, 25, and 33), with major surfaces of the applied isolation material and the buffer film layer in contact. Fig. 7; page 5, lines 17-19; page 7, lines 17-21. The isolation material also fills the trench. *See id*; independent claims 1, 11, 25, and 33. The isolation material may be annealed to densify the same. Claims 5, 15, 28, and 36; page 5, lines 19-21; page 7, lines 21-26.

Thereafter, a portion of the isolation material layer that is located above the buffer film layer may be removed. Independent claims 1, 11, 25, and 33; Fig. 8; page 5, lines 21-25; page 7, line 27, to page 8, line 1. The buffer film layer may also be removed. Independent claims 1, 11, 25, and 33; Fig. 9; page 5, lines 25-26; page 8, lines 1-3. The isolation material forms a shallow trench isolation (STI) structure which has a capped appearance. Independent claims 11 and 33; *see also* Fig. 10; page 5, line 26, to page 6, line 2; page 8, lines 3-7. The capped portion of the STI structure may extend over an upper surface of the semiconductor substrate (claims 16 and 37), for example, a distance of about 50 Å to about 150 Å (claims 17 and 38). Page 8, lines 7-9.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) Whether claims 1-4, 11-14, 16, 25-27, 33-35, and 37 are allowable under 35 U.S.C. § 103(a) for reciting subject matter which is nonobvious and, thus, patentable over the subject matter taught in U.S. Patent 5,712,185 to Tsai et al. (hereinafter "Tsai"), in view of teachings from U.S. Patent 4,835,584 to Lancaster (hereinafter "Lancaster");

(B) Whether, under 35 U.S.C. § 103(a), the subject matter to which claims 17 and 38 are directed is nonobvious and, thus, patentable over the subject matter taught in Tsai, in view of the teachings of Lancaster and, further, in view of the Examiner's Comment; and

(C) Whether claims 5, 15, 28, and 36 are allowable under 35 U.S.C. § 103(a) for being drawn to subject matter that is nonobvious and, thus, patentable over teachings from Tsai, in view of teachings from Lancaster and, further, in view of the teachings of Lee, HS, et al., "An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation (STI)," 1996 IEEE Symposium on VLSI Technol. Dig. of Technical Papers, pages 158-59 (hereinafter "Lee").

VII. ARGUMENT

Claims 1-5, 11-17, 25-28, and 33-38 have been rejected under 35 U.S.C. § 103(a).

A. APPLICABLE LAW

The standard for establishing, maintaining, and upholding a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In determining whether a *prima facie* case of obviousness exists, the teachings of the references must be considered in their entireties. M.P.E.P. § 2141.02.

B. ART RELIED UPON

Tsai

Tsai teaches a process for fabrication isolation structures. The process of Tsai includes forming a trench 38 through a photomask 37, a sacrificial silicon oxide layer 36, a silicon nitride layer 34, and a pad oxide layer 32, and into a silicon substrate 30, as shown in FIGs. 3C and 3D. *See also* col. 2, line 53, to col. 3, line 18. Once the trench 38 is formed, the photomask 37 is removed and the edges of the remainder of the silicon nitride layer 34A are etched back, as depicted by FIG. 3E. *See also* col. 3, lines 9 and 19-33. Thereafter, exposed silicon at the surfaces of the trench 38A is oxidized to form side wall oxidation 39. FIG. 3F; col. 3, lines 34-38. The side wall oxidation 39 relieves defects that are formed in the silicon substrate 30 as the edges of the silicon nitride layer 34A are etched back. Col. 3, lines 34-37.

Lancaster

The teachings of Lancaster are directed to a process for forming a transistor within a trench. That process includes forming an oxide lining 52a within trenches 56 that extend into a silicon substrate 50. FIG. 5D; col. 3, lines 43-45. The oxide lining 52a is purportedly formed to protect the silicon substrate 50 as a silicon nitride mask layer 53 is subsequently removed. Col. 3, lines 39-49; FIG. 5E. Notably, the *entire* silicon nitride mask layer 53 is removed. *Id.*

The oxide lining 52a, which is included merely for the sake of providing etch selectivity to prevent enlargement of the trenches 56 during removal of the silicon nitride mask layer 53 (col. 3, lines 43-45), is removed following removal of the silicon nitride mask layer 53. Col. 3, lines 46-49 and 54-58.

C. ANALYSIS

1. TSAI IN VIEW OF LANCASTER

Claims 1-4, 11-14, 16, 25-27, 33-35, and 37 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over the subject matter taught in U.S. Patent 5,712,185 to Tsai et al. (hereinafter "Tsai"), in view of teachings from U.S. Patent 4,835,584 to Lancaster (hereinafter "Lancaster").

It is respectfully submitted that there are at least three reasons that a *prima facie* case of obviousness has not been established against any of claims 1-4, 11-14, 16, 25-27, 33-35, or 37.

It is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine teachings from Tsai and Lancaster in the manner that has been asserted. In particular, Lancaster teaches a transistor gate fabrication process in which trenches are lined with a sacrificial oxide 52a prior to removing a silicon nitride layer 53, whereas the teachings of Tsai are drawn to a process for forming a trench isolation structure which includes lining trenches side wall oxidation 39 to relieve defects that occur as the edges of the silicon nitride layer 34A are etched back (col. 3, lines 34-37). Although, according to the Examiner, the process of Lancaster would have been know at the time the process disclosed in Tsai was developed, Tsai teaches that, rather than lining the trenches before removing silicon nitride, the trenches are lined following

etch-back of silicon nitride. Accordingly, the inventors of Tsai, who are presumably of at least ordinary skill in the art, did not consider pre-coating the trenches as an option at the time the application which ultimately issued as Tsai was filed. Thus it appears from the teachings of Tsai that, before the earliest priority date for the '959 Application, one of ordinary skill in the art would not have been motivated to incorporate teachings from Lancaster into the process of Tsai.

Furthermore, the radical, complete silicon nitride removal process taught in Lancaster would likely damage the silicon substrate. In fact, Lancaster teaches that the substrate must be protected (with sacrificial oxide 52a) prior to removing the silicon nitride film 53. The number of defects that occur in the descuming process taught in Tsai, in which very small portions of the silicon nitride layer are removed, is correspondingly small. As the subsequent formation of side wall oxidation on the walls of trenches formed in the silicon substrate is sufficient to relieve these defects, one or ordinary skill in the art (including Tsai) would see no reason to form the side wall oxidation 39 before the descuming process.

Additionally, it is respectfully submitted that the references teach away from the asserted combination. Lancaster teaches complete removal of a silicon nitride layer prior to filling trenches. This teaching is inconsistent with Tsai's teaching that a silicon nitride layer remain in place until after trenches are filled to "act[] as an end point detecting layer during [a] CMP process" in which dielectric, trench-filling material that overlies the plane of the silicon nitride layer is removed. Tsai, col. 3, lines 51-56; FIG. 3G.

Moreover, by teaching the complete removal of a silicon nitride layer before forming a transistor gate structure therein, Lancaster teaches away from a method in which portions of a

silicon nitride layer remain as dielectric material is introduced into a trench to form an isolation structure therein, as recited in claims 1-4, 11-14, 16, 25-27, 33-35, and 37.

Therefore, it does not appear that, without the benefit of hindsight that has been provided to the Examiner by the disclosure and claims of the '959 Application, one of ordinary skill in the art would have been motivated to combine teachings from Tsai and Lancaster in the manner that has been asserted.

It is, therefore, respectfully submitted that the teachings of Tsai and Lancaster do not support a *prima facie* case of obviousness against any of claims 1-4, 11-14, 16, 25-27, 33-35, or 37. Accordingly, under 35 U.S.C. § 103(a), each of these claims is drawn to subject matter which is allowable over the teachings of Tsai and Lancaster, taken either separately or together.

2. TSAI, LANCASTER, AND THE EXAMINER'S COMMENT

Claims 17 and 38 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is allegedly unpatentable over that taught in Tsai, in view of the teachings of Lancaster and, further, in view of the Examiner's Comment.

Claim 17 is allowable, among other reasons, for depending indirectly from claim 11, which is allowable.

Claim 38 is allowable, among other reasons, for depending indirectly from claim 33, which is allowable.

3. TSAI, LANCASTER, AND LEE

Claims 5, 15, 28, and 36 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over that the subject matter taught in Tsai, in view of teachings from Lancaster and, further, in view of the teachings of Lee, HS, et al., "An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation (STI)," 1996 IEEE Symposium on VLSI Technol. Dig. of Technical Papers, pages 158-59.

Claims 5, 15, 28, and 36 are allowable, among other reasons, for depending directly from claims 1, 11, 25, and 33, respectively, which are allowable.

VIII. CLAIMS APPENDIX

The current status of each claim that has been introduced into the '783 Application is set forth in the CLAIMS APPENDIX to this Appeal Brief.

IX. EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132. Accordingly, no EVIDENCE APPENDIX accompanies this Appeal Brief.

X. RELATED PROCEEDINGS APPENDIX

No decisions have been rendered by the Board or any court in a related application. Therefore, this Appeal Brief is not accompanied by a RELATED PROCEEDINGS APPENDIX.

XI. CONCLUSION

It is respectfully submitted that:

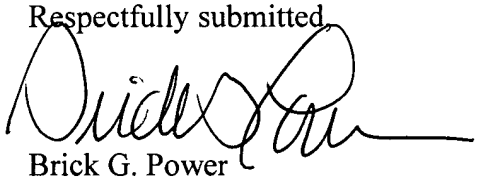
(A) Claims 1-4, 11-14, 16, 25-27, 33-35, and 37 are allowable under 35 U.S.C. § 103(a) for reciting subject matter which is nonobvious and, thus, patentable over the subject matter taught in Tsai, in view of teachings from Lancaster;

(B) Under 35 U.S.C. § 103(a), the subject matter to which claims 17 and 38 are directed is nonobvious and, thus, patentable over the subject matter taught in Tsai, in view of the teachings of Lancaster and, further, in view of the Examiner's Comment; and

(C) Claims 5, 15, 28, and 36 are allowable under 35 U.S.C. § 103(a) for being drawn to subject matter that is nonobvious and, thus, patentable over teachings from Tsai, in view of teachings from Lancaster and, further, in view of the teachings of Lee.

Therefore, it is respectfully requested that the final rejections of claims 1-5, 11-17, 25-28, and 33-38 be withdrawn and that each of these claims be allowed.

Respectfully submitted,



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CLAIMS APPENDIX

1. (Currently amended) A method of forming an isolation structure for a semiconductor device, comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench;

selectively etching a portion of said buffer film layer after the oxide layer has been formed;

applying a layer of isolation material over said buffer film layer and filling said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

2. (Original) The method of claim 1, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

3. (Previously presented) The method of claim 1, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

4. (Previously presented) The method of claim 3, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

5. (Original) The method of claim 1, further including annealing said isolation material layer.

6-10 (Canceled)

11. (Currently amended) A method of forming a capped shallow trench isolation structure for a semiconductor device, comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench sidewalls and said trench bottom;

selectively etching a portion of said buffer film layer after the oxide layer has been formed to expose portions of an upper surface of said dielectric layer adjacent to an upper edge of said trench;

applying a layer of isolation material over said buffer film layer, said isolation material also substantially filling said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

12. (Original) The method of claim 11, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

13. (Previously presented) The method of claim 11, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

14. (Previously presented) The method of claim 13, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

15. (Original) The method of claim 11, further including annealing said isolation material layer.

16. (Previously presented) The method of claim 11, wherein said capped shallow trench isolation structure includes ledges which extend a distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

17. (Original) The method of claim 16, wherein said ledges extend over said upper surface of said semiconductor substrate between about 50 and 150Å.

18-24 (Canceled)

25. (Currently amended) A method of forming an isolation structure on a semiconductor device structure that includes a semiconductor substrate, a dielectric layer, and a buffer film layer, a trench extending through said buffer film layer and said dielectric layer and into said semiconductor substrate, and an oxide layer located on portions of said semiconductor substrate within said trench, the method comprising:

selectively etching a portion of said buffer film layer;

applying a layer of isolation material over said buffer film layer, said isolation material substantially filling said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

26. (Previously presented) The method of claim 25, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

27. (Previously presented) The method of claim 26, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

28. (Original) The method of claim 25, further including annealing said isolation material layer.

29-32 (Canceled)

33. (Currently amended) A method of forming a capped shallow trench isolation structure for a semiconductor device structure that includes a semiconductor substrate, a dielectric layer, and a buffer film layer, a trench extending through said buffer film layer and said dielectric layer and into said semiconductor substrate, and an oxide layer located on portions of said semiconductor substrate within said trench, the method comprising:

selectively etching a portion of said buffer film layer to expose portions of an upper surface of said dielectric layer adjacent an upper edge of said trench;

applying a layer of isolation material over said buffer film layer, said isolation material substantially filling said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

34. (Previously presented) The method of claim 33, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

35. (Previously presented) The method of claim 34, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

36. (Original) The method of claim 33, further including annealing said isolation material layer.

37. (Previously presented) The method of claim 33, wherein said capped shallow trench isolation structure includes ledges which extend a distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

38. (Original) The method of claim 37, wherein said ledges extend over said upper surface of said semiconductor substrate between about 50 and 150Å.